UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/724,585	11/28/2000	John Mark Beardslee	BRIDP004	7620

7590 04/22/2004

JAMES C. SCHELLER, JR.
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	10

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/724,585	BEARDSLEE ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2, 4, 5, 6 and 9*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 of the application have been examined.

Information Disclosure Statement

2. Acknowledgment is made of the information disclosure statements filed on February 26, 2001, April 4, 2001, August 8, 2001, May 20, 2002, November 7, 2002 and January 1, 2004 together with copies of the patents and papers. The patents and papers have been considered in reviewing the claims.

Drawings

3. The drawings submitted on March 7, 2001 are accepted.

Claim Objections

4. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

5. Claims 10 and 21-24 are objected to because of the following informalities:

Claim 10, Lines 2-4, "wherein the activating (a) operates to enable a user to set one or more trigger conditions from the trigger conditions available by the

instrumentation circuitry" appears to be incorrect and it appears that it should be "wherein the activating (a) operates to enable a user to set one or more trigger conditions from the trigger conditions available via the instrumentation circuitry".

Claim 21, Lines 4-5, "(a) activating certain aspects available for examining or modifying by the instrumentation circuitry" appears to be incorrect and it appears that it should be "(a) activating certain aspects available for examining or modifying via the instrumentation circuitry".

Claims objected to but not specifically addressed are objected to based on their dependency to an objected claim.

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

7. Claims 1-12, 14 and 20-23 are rejected under 35 U.S.C. § 102(e) as being anticipated by **Gregory et al. (GR)** (U.S. Patent 5,937,190).

7.1 **GR** teaches architecture and method for a hardware description language source level analysis and debugging system. Specifically, as per claim 1, **GR** teaches a method for debugging an electronic system having instrumentation circuitry included therein, wherein the electronic system is described with an HDL (CL1, L17-19; CL9, L7-25); the method comprising:

(a) activating certain design visibility, design patching or design control aspects of the instrumentation circuitry available for examining or modifying the electronic system via the instrumentation circuitry (CL9, L38-41; CL9, L26-29);

(b) determining configuration information based on the certain design visibility, design patching or design control aspects that are activated (CL9, L38-41; CL9, L26-29);

(c) configuring the instrumentation circuitry in accordance with the configuration information (CL9, L10-20);

(d) receiving debug data from the configured instrumentation circuitry operating within the integrated circuit product (CL9, L42-46);

e) translating the debug data into HDL-related debug information (CL9, L42-46); and

(f) relating the HDL-related debug information to the HDL description (CL8, L43-45).

Per Claims 2-4: **GR** teaches HDL description is a high-level HDL description (CL3, L12-18; CL19, L31-36);

the HDL-related debug information is described in a high-level HDL (CL5, L16-18; CL1, L45-47; CL20, L15-19); and

the translating (e) is performed automatically (CL9, L7-14).

Per Claims 5-7: **GR** teaches that the method operates without any requirement for a test bench (CL9, L7-14);

the debug data includes at least status information or sampling data (CL9, L47-51); and

the activating (a) operates to enable a user to activate the certain design visibility, design patching or design control aspects (CL9, L38-41; CL9, L26-29).

Per Claims 8-10: **GR** teaches that the activating (a) is performed using a graphical user interface (Fig 43);

(g) displaying the high-level HDL description with the HDL-related debug information related thereto (CL8, L38-40; CL9, L42-46); and

the design control aspects include trigger conditions, and wherein the activating (a) operates to enable a user to set one or more trigger conditions from the trigger conditions available by the instrumentation circuitry (CL9, L5-9).

Per Claims 11-12: **GR** teaches that the electronic system comprises an integrated circuit (CL1, L16-19); and

the electronic system comprises a programmable integrated circuit (CL1, L16-19; CL10, L47-50).

Per Claim 14: **GR** teaches (g) interacting with a functional simulator which simulates a portion of the electronic system (CL5, L39-49).

7.2 As per claim 21, **GR** teaches a method for debugging an integrated circuit product having instrumentation circuitry included therein, wherein the integrated circuit product was designed with a high-level HDL description (CL1, L17-19; CL9, L7-25; CL3, L12-18; CL19, L31-36); the method comprising:

(a) activating certain aspects available for examining or modifying by the instrumentation circuitry (CL9, 38-41; CL9, L26-29);

(b) determining configuration information based on the certain aspects that are activated (CL9, L26-29; CL9, L38-41);

(c) configuring the instrumentation circuitry in accordance with the configuration information (CL9, L10-20);

(d) receiving debug data from the configured instrumentation circuitry operating within the integrated circuit product (CL9, L42-46);

(e) translating the debug data into HDL-related debug information (CL9, L42-46);

(f) relating the HDL-related debug information to the high-level HDL description (CL8, L43-45);

(g) thereafter retrieving circuit status information for the integrated circuit product via the instrumentation circuitry (CL9, L47-51);

(h) displaying state information concerning the integrated circuit product based on the retrieved circuit status information (CL8, L38-40; CL9, L42-46).

Per Claims 22-23: **GR** teaches that the HDL-related debug information is described in a high-level HDL (CL5, L16-18; CL1, L45-47; CL20, L15-19); and

relating the state information to the high-level HDL description (CL8, L38-40; CL9, L42-46); and

displaying the high-level HDL description of the integrated circuit product with the state information related thereto (CL8, L38-40; CL9, L42-46).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

9. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Gregory et al. (GR)** (U.S. Patent 5,937,190) in view of **Mason et al. (MA)** (U.S. Patent 6,272,451).

10.1 As per claim 13, **GR** teaches the method of claim 1. **GR** does not expressly teach that the electronic system includes a hardware portion and a software portion, and wherein the method further comprises (g) interacting with a software debugger which debugs the software of the electronic system. **MA** teaches that the electronic system includes a hardware portion and a software portion (CL9, L18-23; CL9, L46-51); and wherein the method further comprises (g) interacting with a software debugger which debugs the software of the electronic system (CL9, L46-51), because that allows integrating the hardware and software portions into an environment for easy product development that accelerates the designer's time to market and allows the designer to do extensive 'what if' analysis between the hardware and software aspects of the design very early in the design process (CL9, L23-29). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **GR** with the method of **MA** that included the electronic system including a hardware portion and a software portion, and wherein the method further comprised (g) interacting with a software debugger which debugged the software of the electronic system. One would be motivated because that would allow integrating the hardware and software portions into an environment for easy product development that accelerated the designer's time to market and would allow the designer to do extensive 'what if' analysis between the hardware and software aspects of the design very early in the design process.

11. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Gregory et al. (GR)** (U.S. Patent 5,937,190) in view of **Mann (MAN)** (U.S. Patent 6,272,451).

11.1 As per claim 15, **GR** teaches the method of claim 1. **GR** does not expressly teach that the electronic system is operated in its target environment and running at its target speed during the debugging. **MAN** teaches that the electronic system is operated in its target environment and running at its target speed during the debugging (CL5, L57 to CL6, L13), because that allows for the capture and display of signals present on address and data buses within the target system using a logic analyzer or other equipment (CL6, L10-13). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **GR** with the method of **MAN** that included the electronic system being operated in its target environment and running at its target speed during the debugging. One would be motivated because that would allow for the capture and display of signals present on address and data buses within the target system using a logic analyzer or other equipment.

12. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gregory et al. (GR)** (U.S. Patent 5,937,190) in view of **Rhim et al. (RH)** (U.S. Patent 6,006,022).

12.1 As per claim 16, **GR** teaches the method of claim 14. **GR** does not expressly teach that the target environment includes real-time characteristics. **RH** teaches that the target environment includes real-time characteristics (CL14, L22-33), because that allows the software model to

model internal states and custom logic with both forward and backward execution based on HDL description and allows the designer to debug both the hardware ad software running together and perform system analysis functions (CL14, L26-30 and L39-41). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **GR** with the method of **RH** that included the target environment including real-time characteristics. One would be motivated because that would allow the software model to model internal states and custom logic with both forward and backward execution based on HDL description and would allow the designer to debug both the hardware ad software running together and perform system analysis functions.

12.2 As per claim 17, **GR** teaches the method of claim 1. **GR** does not expressly teach that the while debugging the electronic system, the electronic system is operating in its target environment. **RH** teaches that while debugging the electronic system, the electronic system is operating in its target environment (CL14, L30-33; CL14, L52-54), because that allows the software model to model internal states and custom logic with both forward and backward execution based on HDL description and allows the designer to debug both the hardware ad software running together and perform system analysis functions (CL14, L26-30 and L39-41). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **GR** with the method of **RH** that included while debugging the electronic system, the electronic system operating in its target environment. One would be motivated because that would allow the software model to model internal states and custom logic with both

forward and backward execution based on HDL description and would allow the designer to debug both the hardware ad software running together and perform system analysis functions.

13. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Gregory et al. (GR)** (U.S. Patent 5,937,190) in view of **Smith et al. (SM)** (U.S. Patent 6,353,906).

13.1 As per claim 18, **GR** teaches the method of claim 1. **GR** does not expressly teach that the debugging operates to identify at least one fault of the electronic system. **SM** teaches that the debugging operates to identify at least one fault of the electronic system (CL5, L12-13), because identification of faults is very critical in debugging the ASIC design, since these types of circuits are difficult to design and verify (CL5, L12-16). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **GR** with the method of **SM** that included the debugging operating to identify at least one fault of the electronic system. One would be motivated because identification of faults is very critical in debugging the ASIC design, since these types of circuits are difficult to design and verify.

14. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Gregory et al. (GR)** (U.S. Patent 5,937,190) in view of **Smith et al. (SM)** (U.S. Patent 6,353,906), and further in view of **Baxter et al. (BA)** (U.S. Patent 6,625,787).

14.1 As per claim 19, **GR** and **SM** teach the method of claim 18. **GR** does not expressly teach that the at least one fault is selected from the group consisting of: specification error, design

error, tool error, device driver error, timing error, manufacturing fault, and environment error. **BA** teaches that the at least one fault is selected from the group consisting of: specification error, design error, tool error, device driver error, timing error, manufacturing fault, and environment error (CL3, L53-57), because the timing errors can be identified by simulating the circuit operation and monitoring the results at selected circuit nodes; the test engineers can then identify the problem paths and then change the HDL description to alter the offending paths (CL3, L37-42). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **GR** with the method of **BA** that included the at least one fault selected from the group consisting of: specification error, design error, tool error, device driver error, timing error, manufacturing fault, and environment error. One would be motivated because the timing errors could be identified by simulating the circuit operation and monitoring the results at selected circuit nodes; the test engineers could then identify the problem paths and then change the HDL description to alter the offending paths.

15. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Gregory et al. (GR)** (U.S. Patent 5,937,190) in view of **Mann (MAN)** (U.S. Patent 6,272,451), and further in view of **Snyder (SN)** (U.S. Patent 5,859,993).

15.1 As per claim 24, **GR** teaches the method of claim 21. **GR** does not expressly teach that the state information includes signal values for signals. **MAN** teaches that the state information includes signal values for signals (CL6, L10-13), because that allows capture and display of signals present in the integrated circuit and the address and data buses within the target system

(CL6, L10-13). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **GR** with the method of **MAN** that included the state information including signal values for signals. One would be motivated because that would allow capture and display of signals present in the integrated circuit and the address and data buses within the target system.

GR does not expressly teach that the relating operates to relate the signal values to HDL identifiers within the high-level HDL description that correspond to the signals. **SN** teaches that the relating operates to relate the signal values to HDL identifiers within the high-level HDL description that correspond to the signals (CL5, L17-29), because the design of the circuit is implemented in HDL using HDL identifiers (CL6, L10-13). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **GR** with the method of **MAN** that included the relating operating to relate the signal values to HDL identifiers within the high-level HDL description that corresponded to the signals. One would be motivated because the design of the circuit was implemented in HDL using HDL identifiers.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
April 15, 2004

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER